7th International Conference on Modelling, Identification and Control (ICMIC 2015)
Sousse, Tunisia - December 18-20, 2015

Catastrophic Faults Detection of Analog Circuits

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Abstract— **In this paper, a new test technique of analog circuits using time mode simulation is proposed for the single catastrophic faults detection in analog circuits. This test process is performed to overcome the problem of catastrophic faults being escaped in a DC mode test applied to the inverter amplifier in previous research works. The circuit under test is a second-order low pass filter constructed around this type of amplifier but performing a function that differs from that of the previous test. The test approach performed in this work is based on two key- elements where the first one concerns the unique square pulse signal selected as an input vector test signal to stimulate the fault effect at the circuit output response. The second element is the filter response conversion to a square pulses sequence obtained from an analog comparator. This signal conversion is achieved through a fixed reference threshold voltage of this comparison circuit. The measurement of the three first response signal pulses durations is regarded as fault effect detection parameter on one hand, and as a fault signature helping to hence fully establish an analog circuit fault diagnosis on another hand. The results obtained so far are very promising since the approach has lifted up the fault coverage ratio in both modes to over 90% and has revealed the harmful side of faults that has been masked in a DC mode test.**

Keywords— **catastrophic faults, analog circuits, fault detection**

I. INTRODUCTION

The level of analog circuits fault diagnosis is still not sufficient despite of continuous research development in this field, and this is due particularly to the limited measurement accessibility of circuits. It follows from the fact that components of analog circuits have continuous values varying within the interval of $[0, \infty]$, where the extreme values 0 and ∞ representing catastrophic faults can consequently change the topology of the circuit. In addition, stimulation and response signals are also continuous and they can assume the shape of any function. Moreover, problems of fault diagnosis are also caused by the presence of component tolerances and circuit nonlinearities [1].

Analog fault diagnosis has been addressed by two general methods [2] simulate-before-test (SBT) and simulate-after-test (SAT). The first is based on the use of fault dictionary, which contains the circuit responses from simulation process of different predefined faults. The second uses measurements to compute the circuits' parameters from solving a set of fault diagnosis equations. All computations occur after measurements are acquired.

In many research works [1], the main factors that make analog circuit diagnosis difficult can be summarized as follows: analog circuits are frequently nonlinear, include noise and have parameter values that vary widely. Another major problem faced in a testing process is today's analog circuits' complexity. This is remarked by the considerable amount of their constructing components, the huge amount of their parameters, the unknown values of the actual component which differ from the nominal values the limited accessibility to their internal components etc.

Faults in analog circuits can be categorized as catastrophic and parametric [6]. Catastrophic faults are open and short circuits, caused by unexpected and large variations of components' values. The parametric faults are reported to the circuit functionality. Thus, the value of parameters deviates continuously with time or with environmental conditions to an unacceptable value [3].

Analog fault diagnosis usually consists of three stages which respectively address three important problems in the analog testing and diagnosis:

- Fault detection: during that we have to find out if the circuit under test is faulty or not;
- Fault location: which has as purpose to identify where the faulty parameters are;
- Parameter evaluation: to tell how much are the parameter deviations from nominal values.

The faults detection in analog electronic circuits is becoming difficult; one of the major difficulties is due to the limited number of output signals, input and test signals. Beside a test process oriented to circuit failures requires sensitive measurements that depend on test stimuli generation and help to solving the diagnostic process problems. Many approaches mentioned in the literature has proposed either noise signal applied as input stimulus or, ramp signal injected at a power supply rail aiming all of them to an easy fault detection and an effective fault isolation. In this paper, a new technique based on input signal selection is set for detecting catastrophic faults and to contributing as a solver to this problem in analog circuit. .Another objective of this paper to make possible catastrophic faults (i.e. open and short circuits in transistors)

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detection which has been escaped in a DC mode test applied to operational amplifiers in previous works [3].

The present fault detection procedure is performed in a transient mode test where the submitted circuit is a second order low pass filter made of three amplifiers similar in structure to that mentioned in the following section. These circuit's components are the target of this test where the faults are applied singularly at their transistor level and whose effects are stimulated at the circuit output by an input unique square pulse signal. The fault detection parameter is set from the measured durations of the signal pulses obtained at the analog comparator output used as an auxiliary test circuit [1]. This is a signal converter of the filter response to a chain of pulses whose time durations constitute a fault effect observation mean. This testing technique was developed and used in this paper to enable significant fault coverage.

II. Description of the Method

The circuit under test used for the implementation of the diagnostic method is illustrated in figure 1. Its structure scheme is based on operational amplifiers µA741 (AOP) whose electronic configuration is made of NPN and PNP transistors. These transistors are belonging to the FERRANTI company [5] and its equivalent electrical models shown in Figure 3, are also property of this component manufactory. Undetected faults in a previous DC mode test are single faults which deliberately affected the transistors of the inverter amplifier simulated in [3]. These anomalies have been applied singularly in each amplifier (AOP1, AOP2, and AOP3) and their fault effect investigation is carried out at the output filtering circuit. This task has been achieved through a fault simulation process performed in a similar way as done in a circuit design fault-free simulation stage.

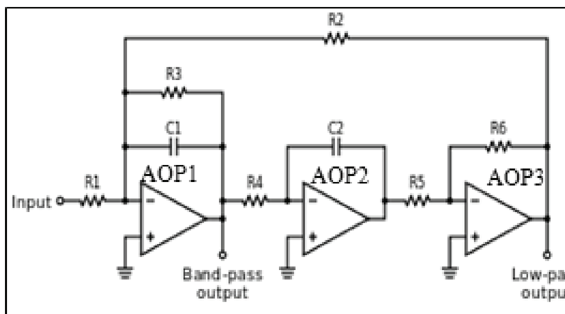


Fig. 1 Analog Circuit Example

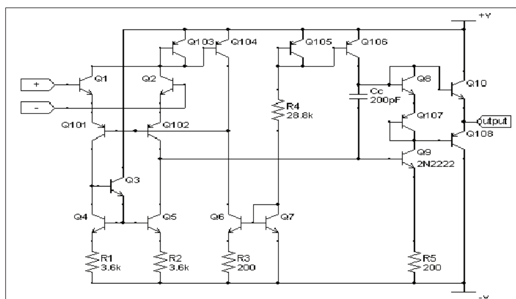
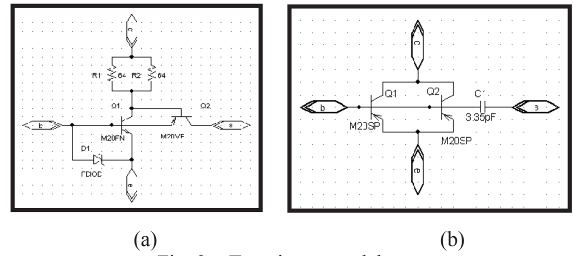


Fig. 2 Internal schematic of µa741.



(a) (b)

Fig. 3 Transistors models.
(a) : NPN transistor, (b) : PNP transistor.

The test method established here has been inspired from several previous works [3][4] and from which useful methods have been combined in order to :

1- Generate and select the efficient signal as input test vector;
2- Insert the analog comparator to meet two requirements:
   - To construct a pulses' sequence with several time durations which are used as fault detection parameters; and a mean of fault coverage ratio improvement
   - To set a fault signature to help in a fault diagnosis process.
3- Make use of a single square pulse and the comparator which are of general use in microprocessor data processing structure. Such feature will allow a possible implementation of this test technique in a built-in self test structure.

The diagram scheme (figure 4) of the testing method consists of four main process elements named as:

- Single square pulse generator that provide the test process with a convenient input test signal (UTS) that convey the fault effect till the circuit output.
- The circuit under test where the amplifying components are the core of hard faults investigation.
- The analog comparator serving as a circuit converter of the C.U.T response (RS) in a square pluses sequence (SPS) shape.
- A unit of pulses time durations measurement (PTDM) helps to get values of these test parameters in order to examine the fault detection signal (FDS) and to provide fault signature data (FSD).

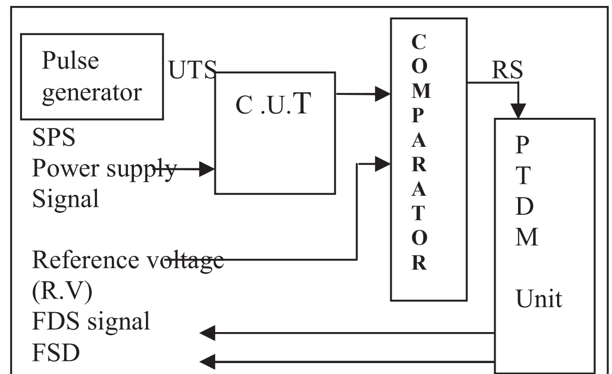


Fig.4 Diagram scheme of the proposed test method

The single analog comparator converts the response of the analog circuit into a set of consecutive (one-by-one) square impulses while comparing it to a reference voltage (RV) of about 50mV. This is necessary for setting the threshold voltage that permits the circuit output to provide four pulses signal only. Henceforth the measurements of these pulses time durations constitute the fault detection and fault effect observation parameters.

A. Faults models

Catastrophic faults are known as hard faults since they result in a change in circuit topology and thus a totally altered circuit function. This kind of faults are generally provoked by various failure mechanisms such as substrate contamination, residues, solder ball lifting and so. Such hard faults are most of them modelled as open and short circuits [2]. The hard faults to which transistors are exposed can be considered as short and open faults, where the first ones are further classified as: (a) emitter to collector, (b) emitter to base (c), and base to collector shorts and are modelled by a small resistance. The latter ones are presented as (a) emitter open, (b) collector open and (c) base open faults. Typically, these faults are modelled by resistive short or open circuit at netlist level. Certain simulation programs require the use of small resistance value (from 0 to 10Ω) to model a short circuit and high resistance value (from 10M Ω to several GΩ) as open circuit model.

The faults escaped in DC mode test are indicated in TABLE I [3] with their respective codes for an easy fault effect study.

TABLE I
ESCAPED FAULTS IN DC MODE TEST OF INVERTING CIRCUIT

Fault code	Element (transistor)	fault
F0	--	Circuit healthy
F1	Q3	Emitter open
F2	Q3	Base open
F3	Q3	Collector open
F4	Q3	Base-emitter shorted
F5	Q4	Collector open
F6	Q4	Emitter-collector shorted
F7	Q4	Base-emitter shorted
F8	Q4	Base-collector shorted
F9	Q5	Emitter open
F10	Q5	Base open
F11	Q5	Collector open
F12	Q5	Base-collector shorted
F13	Q7	Collector open
F14	Q8	Collector open
F15	Q8	Base open
F16	Q101	Collector open
F17	Q103	Collector open
F18	Q105	Collector open
F19	Q107	Base open
F20	Q108	Collector open

B. Idea of the method

From the simulation of the analog circuit represented in Figure. 1 under a unique square pulse input excitation (with a duration time T = 568 ms), we get an analog response that passes several times the level of zero voltage, as shown in figure 5. This response is compared to the above mentioned reference voltage (RV) of the analog comparator. The filtering circuit output delivers a sequence of pulses with different durations t1, t2, t3. We took into account the first three pulses durations (Figure. 6) only in order to ovoid on one hand a huge amount of data that comes out from these time parameters measurement and the process time consumption on the other hand. This is the most important requirement of a test process that should be fulfilled. This operation of simulation has been carried out by use of the efficient electrical simulator OrCad Pspice and repeated over all faulty circuit cases.

III. SIMULATION AND RESULTS

The circuit shown in Figure 1 was simulated using Orcad-Pspice. Operational amplifiers constituting the circuit contain transistors that belong to the FERRANTI Company. The AOPs are under a power supply of +/-5Volts. The faults in table I are individually injected into each of these AOPs while bearing in mind one defect amplifier at a time. The simulation results following this faults investigation are given in tables III, IV and V. These indicate variations on the pulses durations of the analog comparator response depending on the amplifier being concerned and the fault type applied to.

A. Simulation of the circuit under test without faults

In a fault free circuit case, the input signal selected as input test vector has led the filter output to deliver a signal response in a form given in figure 4. This is seen as a pseudo periodic signal which consists of a negative trapezoidal pulse with a - 4V amplitude level followed by a vanishing sine wave.

This response signal applied to the analog comparator circuit is converted to a chain of pulses (SPS signal) whose number is fixed according to the response wave amplitude level that exceeds the RV level of 50mV.

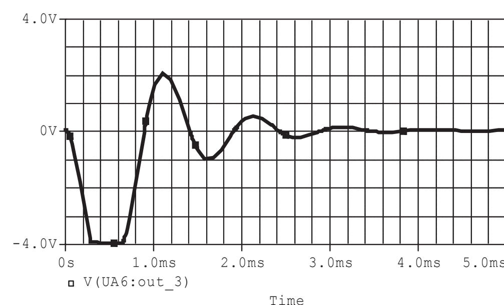


Fig.5 Response of the circuit under test

The SPS signal resulted from simulation is illustrated in figure 6 as a four pulses sequence with different time durations t1,t2,t3 and t4 only, though the last time duration (t4) has been out of concern in our test process due to the raisons of time process claimed before.

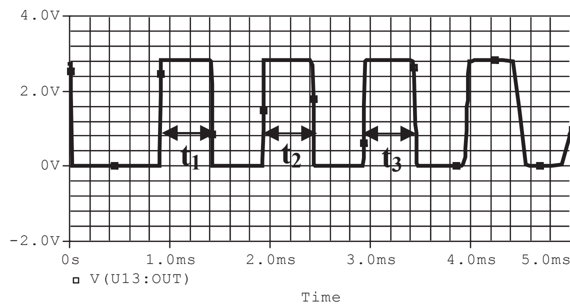


Fig.6 Response of the comparator.

The measured time values are picked up from the simulation results and gathered in a table 2.

TABLE II
PULSES DURATION VALUES

Pulse duration	t1(µs)	t2(µs)	t3(µs)
value	526.04	539.80	631.40

IV. RESULTS INTERPRETATION AND DISCUSSION

In this paper section, the main attention is focused on fault detection ratio and fault signature construction that can evaluate the test process efficiency on one hand and to establish fault diagnosis on another hand. This task is carried out on data collection from the fault simulation results over all faults cases (20 faults) applied to the three operational amplifiers; this has led to 20x3 fault cases to be studied.

The test approach being applied for detecting faults is based on the following assumptions:

- A fault is assumed to be detected if at least one the three selected time durations shows a precise value deviation computed as a difference between the duration nominal value and that of the fault case.;
- The precise deviation for fault detection is set at a ratio over a 10% of a time duration nominal value.
- Under this ratio, the fault is considered as either error of tolerance or undetectable fault.

TABLE III
VARIATION IN THE PULSES DURATION VALUES WHEN FAULTS ARE INJECTED IN AOP1

Faults	Estimated parameters		
	t1(%)	t2(%)	t3(%)
F0	0	0	0
F1	7.16	28.21	No pulse
F2	6.95	28.79	No pulse
F3	2.54	14.69	51.82
F4	7.51	No pulse	No pulse
F5	3.35	40.12	No pulse
F6	9.63	41.59	No pulse
F7	9.15	38.98	No pulse
F8	1.53	2.50	2.58
F9	5.50	17.19	55.91
F10	1.16	5.39	11.75
F11	6.03	27.92	No pulse
F12	2.28	7.43	No pulse
F13	1.52	6.61	No pulse
F14	0.51	4.06	12.50
F15	0.83	8.58	No pulse
F16	2.65	5.93	28.02
F17	9.27	38.96	No pulse
F18	3.65	17.84	No pulse
F19	1.27	7.32	28.01
F20	10.23	39.85	No pulse

TABLE IV
VARIATION IN THE PULSES DURATION VALUES WHEN FAULTS ARE INJECTED IN AOP2

Faults	Estimated parameters		
	t1(%)	t2(%)	t3(%)
F0	0	0	0
F1	1.31	75.02	No pulse
F2	4.66	14.08	No pulse
F3	2.77	9.15	No pulse
F4	No pulse	No pulse	No pulse
F5	1.49	23.30	No pulse
F6	4.77	21.47	No pulse
F7	4.77	24.62	No pulse
F8	No pulse	No pulse	No pulse
F9	2.71	5.08	No pulse
F10	3.11	2.96	4.28
F11	1.52	18.25	No pulse
F12	2.79	4.56	5.29
F13	0.63	0.82	10.03
F14	0.44	0.70	2.80
F15	0.64	1.06	8.20
F16	0.47	5.24	No pulse
F17	5.80	24.58	No pulse
F18	92.88	No pulse	No pulse
F19	0.47	5.24	No pulse
F20	5.93	24.54	No pulse

TABLE V
VARIATION IN THE PULSES DURATION VALUES WHEN FAULTS ARE INJECTED IN AOP3

Faults	Estimated parameters		
	t1(%)	t2(%)	t3(%)
F0	0	0	0
F1	0,34	1.17	2.80
F2	0,81	2.20	2.58
F3	0,03	0.31	0.74
F4	0,56	0.22	0.30
F5	0,28	2.30	1.77
F6	1,42	2.32	1.92
F7	1,38	2.32	1.92
F8	1,62	3.30	1.12
F9	1,81	3.01	24.41
F10	0,72	2.89	0.79
F11	1,50	3.52	1.01
F12	1,31	0.78	1.01
F13	0,62	3.32	0.79
F14	0,39	2.83	2.58
F15	1,01	0.00	0.79
F16	0,37	0.13	19.26
F17	0,58	3.37	1.01
F18	1,57	0.61	0.11
F19	0,37	0.13	0.65
F20	0,18	0.61	1.65

The analysis of data recorded in table III lets appear different time durations (t1, t2, and t3) values for almost all the faults that can attain the AOP1circuit. The t1 parameter used as a first detection criterion has led the fault coverage ratio to 1/20 (5% of detected faults).The second and the third time duration have respectively conducted to 12/20 (58%) and 13/20 (62%) of detected faults which are seen as improved fault coverage proper to the first amplifier. A combination of these three time criteria has consequently conducted to a better fault coverage improvement since a 20/20 fault coverage ratio is achieved (100% of faults were detected).

In the faults' case applied to the second AOP, the recorded fault effect data in table IV shows a 11/20 as fault coverage ratio acquired with the combined three times criteria. This corresponds to a 51% of detected faults. In the last faults 'case dealing with the third amplifier, two faults are detected only with the third time criterion which unfortunately has led to the lowest fault coverage: 1% of detected faults is achieved. From these results, it can be remarked that changing the function of the amplifier can alter positively or subjectively the fault coverage value. On the other hand, all the tested amplifiers gathered have amazingly contributed to highest fault coverage value of 100% as mentioned in table VI.

From Tables III, IV and V, we can classify the faults in three categories: the first category contains faults that completely change the response of the comparator (D), the second category contains faults that do not change the shape of the comparator response but act on the pulse durations (deviation of the pulses durations exceeding 10%).The third category gather undetected faults (U) (deviation of the durations is less than 10% pulse), these faults can be assumed as tolerance faults. This technique has allowed us to improve the coverage of catastrophic faults raising it to 100%

TABLE VI
DETECTED AND UNDETECTED FAULTS

Faults	AOP1	AOP2	AOP3	Circuit under test
F1	D	D	U	D
F2	D	D	U	D
F3	D	D	U	D
F4	D	D	U	D
F5	D	D	U	D
F6	D	D	U	D
F7	D	D	U	D
F8	U	D	U	D
F9	D	D	D	D
F10	D	U	U	D
F11	D	D	U	D
F12	D	D	U	D
F13	D	U	U	D
F14	D	U	U	D
F15	D	D	U	D
F16	D	D	D	D
F17	D	D	U	D
F18	D	D	U	D
F19	D	D	U	D
F20	D	D	U	D

V. CONCLUSIONS

In this paper, we have presented a methodology for detecting catastrophic faults in an analog circuit based on operational amplifiers µA741 in time domain test mode. The circuit under test is a second order low pass filter built with three amplifiers of the same internal structure. The faults induced to it are those escaped from a DC mode test carried out on an inverter amplifier as treated in anterior research works. The 20th faults being investigated in each amplifier are all of them detected at the overall circuit output (circuit under test). This has been achieved by combining the fault coverage reached with the three amplifiers submitted to test process on one hand, and three pulse time durations used as test detection parameters. The concluding remarks we draw from the work results acquaint that changing test mode or a circuit function of an analog circuit will aid in fault detection maximization

Looking ahead, other test modes will be used in the future in order to ensure fault detection improvement by minimizing the ambiguity in faults groups to serve as their isolation or their location mean.

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